ABSTRACT

An integrated dynamic memory includes memory cells which are combined to form individual independently addressable units, and a control circuit for controlling a refresh mode for the memory cells. The memory cells can have their memory cell content refreshed. The control circuit is designed such that one or more units of memory cells can be subject to a refresh mode in parallel in a refresh cycle. The control circuit sets a number of memory cell units, which are to be refreshed in parallel in a refresh cycle based on a temperature reference value. A maximum possible operating temperature for a memory chip can be increased without additional restrictions on memory access.